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Heppler

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[54] METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS

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[58] Field of Search ..... 209/552, 559, 571, 573, 209/574, 575, 655, 911; 324/158 F; 198/346.2, 346.3, 360

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[57] ABSTRACT

There is an IC (integrated circuit) testing device 11 that receives singulated ICs from a singulation station's bottom table 44, where an IC 15 has slid down onto loading ramp or track 16. The IC will slide into test station 18, where stop pin 22 has been inserted to stop the IC in DUT (device under test) station 20. In the DUT station, the IC is securely held in position by an extractor bar 26, insertion bar 28, and a part guide 24. Thereby, test cite station 18 will move downward and insert IC 15 into testing socket 30. After testing the IC, testing station 18 returns upward with the IC in the same secured position. Pin 22 will be removed to allow the IC to slide into part holding station 31. If the IC was not defective, pin 32 will be removed to allow the IC to slide onto track 36 of the IC separator station 34. While the test cite station 18 is in the up position a second IC is slid along track 16 and loaded into DUT cite 20 being readied for th next test cycle. However, if the first IC was found to be defective, pin 32 will be positioned so as to stop the IC from sliding onto track 36. Thereby, the test cite 18 will proceed to the down position to test the second IC, and simultaneously pin 32 will be removed to now allow the defective IC to slide onto track 38. The second IC has now completed its testing and is ready to proceed to the remainder of the cycle.

6 Claims, 4 Drawing Sheets